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Application No. 09/392,034	Filing Date September 8, 1999	Examiner Anh D. Mai	Customer No. 022901	Group Art Unit 2814

Invention: **METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH**

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Docket No. 11675.119.1.1

In Re Application Of: **Fernando Gonzalez et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/392,034	September 8, 1999	Anh D. Mai	022901	2814	9481

Invention: **METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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William J. Athay
Attorney for Applicant
Registration No. 44,515

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PATENT APPLICATION
Docket No.: 11675.119.1.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:		
	Fernando Gonzalez et al.	
Serial No.:	09/392,034	
Filed:	September 8, 1999	Art Unit 2814
For:	METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH	
Confirmation No.:	9481	
Examiner:	Anh D. Mai	

BRIEF OF APPELLANTS

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants, Fernando Gonzalez, David Chapek, and Randhir P.S. Thakur, have filed a timely Notice of Appeal from the action of the Examiner in finally rejecting all of the claims in this application. This brief is being filed under the provisions of 37 C.F.R. § 1.192. The filing fee of $500.00, as set forth in 37 C.F.R. § 1.17(c) is submitted herewith.

REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., by way of assignment from Fernando Gonzalez, David Chapek, and Randhir P.S. Thakur, who are the named inventors and are captioned in the present brief. The assignment documents were recorded at Reel No. 8488, Frame 0262 in the United States Patent and Trademark Office on March 25, 1997.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1, 3-27, 31-40, 42, and 43 are pending and appealed in the present application. Claims 2, 28-30, and 41 have been cancelled.

STATUS OF AMENDMENTS

All amendments have been previously entered.

SUMMARY OF INVENTION

The present invention relates to a method for forming an isolation trench structure on a semiconductor substrate. The inventive method forms and fills the isolation trench without causing deleterious topographical depressions in the upper surface of the fill material in the isolation trench, while substantially preventing contact between layers overlying the fill material of the isolation trench and the active area of the semiconductor substrate. Page 5, lines 2-8. By

avoiding such deleterious topographical depressions and the exposure of the active area, detrimental charge and current leakage is minimized. *Id.*

In one embodiment, the inventive method of forming an isolation trench comprises forming a pad oxide 14 upon a semiconductor substrate 12 and depositing a first dielectric layer 16 thereupon. Page 5, lines 9-15, Figure 2A. By way of non-limiting example, the first dielectric layer 16 is a nitride layer. The first dielectric layer 16 is patterned and etched with a mask 20 to expose a portion of the pad oxide layer 14 and to protect an active area in the semiconductor substrate 12 that remains covered with the first dielectric layer. Figure 3A. A second dielectric layer 26 is formed substantially conformably over the pad oxide layer 14 and the remaining portions of the first dielectric layer 16. Figure 4A.

A spacer etch is used to form a spacer 28 from the second dielectric layer 26. Page 5, lines 16-24; page 11. lines 12-19; Figure 5A The spacer 28 electrically insulates the first dielectric layer 16. An isolation trench etch follows the spacer etch and creates within the semiconductor substrate 12 an isolation trench 32 that is defined by sidewalls 50 in the semiconductor substrate 12. The spacer 28 formed by the spacer etch facilitates self-alignment of the isolation trench 32 formed by the isolation trench etch. The isolation trench etch can be carried out with the same etch recipe as the spacer etch, or it can be carried out with an etch recipe that is selective to the spacer. Once the isolation trench is formed, an insulation liner 30 on the inside surface of the isolation trench 32 can be optionally formed, either by deposition or by thermal oxidation. Page 12, lines 1-17. The liner 30 preferably has rounded corners. Page 12, lines 10-13

A third dielectric layer 36 is formed substantially conformably over the spacer and the first dielectric layer so as to substantially fill the isolation trench 32 and have a contoured upper

surface. Figure 6A. Topographical reduction of the third dielectric layer 36 follows, preferably so as to planarize the third dielectric layer beginning with the contoured upper surface, for example by chemical mechanical planarizing (CMP). Page 14, lines 14-25. The etch is preferably performed such that insulator island 22 etches faster than isolation film 36.

The topographical reduction of the third dielectric layer may also be carried out as a single etchback step that sequentially removes superficial portions of the third dielectric layer that extend out of the isolation trench. Page 17, lines 8-24. The single etchback also removes portions of the remaining spacer, and removes substantially all of the remaining portions of the first dielectric layer. Preferably, the single etchback will use an etch recipe that is more selective to the third dielectric layer and the spacer than to the remaining portions of the first dielectric layer. The single etchback uses an etch recipe having a selectivity that will preferably leave a raised portion of the third dielectric layer extending above the isolation trench while removing substantially all remaining portions of the first dielectric layer. The resulting structure can be described as having the shape of a nail as viewed in a direction that is substantially orthogonal to the cross section of a word line in association therewith. *See* Figures 8A and 8B.

Several other processing steps are optional in the inventive method. One such optional processing step is the deposition of a polysilicon layer upon the pad oxide layer to act as an etch stop or planarization marker. *See* Figures 2B, 3B, 4B, 5B, 6B, 7B, 8B, and 9B. An additional optional processing step includes implanting doping ions at the bottom of the isolation trench to form a doped trench bottom 34.

ISSUES

1. Whether the specification should be objected to as self-contradicting.

2. Whether the drawings should be objected to under 37 C.F.R. §1.84(p)(4) because the reference characters 14 and 44 are not accurately used.

3. Whether claim 23 recites a limitation not shown in the drawings and the drawings should therefore be objected to under 37 C.F.R. §1.83(a).

4. Whether claims 14-23, 25-27, and 31-40 should be objected to because there is no nexus between cited limitations and other features of the claims.

5. Whether claim 23 should be objected to under 37 C.F.R. § 1.75(c) because it does not limit a prior claim.

6. Whether claim 34 should be objected to for using an incorrect term.

7. Whether claims 1 and 3-6 should be rejected under 35 U.S.C. § 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the invention was filed, had possession of the claimed invention.

8. Whether claims 14-27, 31-40, and 43 should be rejected under 35 U.S.C. § 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the invention was filed, had possession of the claimed invention.

9. Whether claim 23 should be rejected under 35 U.S.C. § 112, first paragraph, for not enabling a person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate with this claim.

10. Whether claims 9, 10, 12, 13, 26, and 27 should be under 35 U.S.C. § 112, second paragraph, for failing to set for the subject matter the Appellants regard as their invention.

11. Whether claims 1, 3-27, and 31-34 are unobvious over U.S. Patent No. 6,097,072 to Omid-Zohoor et al. ("the '072 patent") in view of U.S. Patent No. 5,387,540 to Poon et al. ("*Poon*").

12. Whether claims 35-40, 42, and 43 are obvious over the '072 patent in view of Wolf, "*Silicon Processing for the VLSI Era*" ("*Wolf*").

GROUPING OF CLAIMS

Claims 1 and 3-6 stand or fall together.

Claims 7, 8, and 11 stand or fall together.

Claims 9, 10, 12, and 13 stand or fall together.

Claims 14-22, 25, and 31-33 stand or fall together.

Claim 23 stands or falls by itself.

Claim 24 stands or falls by itself.

Claims 26 and 27 stand or fall together.

Claim 34 stands or falls by itself.

Claims 35-40 stand or fall together.

Claims 42 and 43 stand or fall together.

ARGUMENT

1. The specification is not self contradicting because the term "selective to" consistently means slower.

The specification stands objected to because in various instances it states that the term "selective to" denotes that a particular layer is etched slower while in others it allegedly denotes that a particular layer is etched faster. The Office Action, therefore, concludes that the specification is self-contradicting. Appellants respectfully disagree.

In particular, the Office Action objects to the language at page 14, lines 14-15 of the Specification: "A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, selective to isolation film 36 as compared to insulator island 22." The Office Action alleges this passage suggest that the isolation film is etched faster while the rest of the application states that the isolation film is etched slower.

In context, and as understood throughout the Specification as filed, it is clear that the isolation film 36 is etched slower than the insulator island. For example, at page 15, lines 11-15 the Specification states in part, "Reduced island 52 is preferably removed with an etch that is selective to isolation film 36 and spacer 28, leaving an isolation structure 48 that extends into and above isolation trench 32, forming a nail shaped structure having a head 54 extending above and away from isolation trench 32 upon an oxide layer 44." It is therefore clear that, as used in the specification, the term "selective to" indicates that a material is etched more slowly than other materials. Although the cited ratio of 2:1 may arguably be unclear if read in isolation, in context it is clear that substituting "slower" for "selective" is clear. In other words, the hypothetically rephrased language "A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, **slower** [selective] to isolation film 36 as compared to insulator island 22" is clear and consistent with the above passage, other sections

of the specification and Appellants previous arguments.

Regarding the cited language at page 15, lines 9-10, "Reduced island 52 preferably acts as a partial etch stop" (emphasis added), Appellant respectively notes that reduced island 52 is a *partial* etch stop, not a complete one. Thus, reduced island 52 helps stop the etching, but only partially. In other words, although reduced island 52 etches faster than isolation film 36, it does help stop the overall etching process.

Appellants therefore respectfully request that this objection to the specification be overturned.

2. The drawings should not be objected to under 37 C.F.R. § 1.84(p)(4) because the reference characters 14 and 44 are not misused.

The drawings stand objected to because both reference characters "14" and "44" have been used to designate a "pad oxide layer" in Figures 7B and 8B. Appellants respectfully disagree.

Appellants respectfully note that Figures 7B and 8B depict different steps in the methods of the invention and do not, therefore, necessarily depict identical structures. As noted at page 16, lines 13-14 of the application as filed, reference character "44" is used in conjunction with Figure 8A and refers to a "gate oxide layer 44," which is differentiated from a "pad oxide layer 14." This is consistent with page 19, line 16 of the Specification, wherein a gate oxide layer is formed in the embodiment discussed with Figure 8B. In other words, a gate oxide layer 44 is shown in Figure 8B as intended.

Appellants therefore respectfully request that this objection to the drawings under 37 C.F.R. § 1.83(a) be overturned.

3. The drawings should not be objected to under 37 C.F.R. § 1.83(a) because the limitations of claim 23 are sufficiently illustrated in the figures.

The drawings stand objected to for failing to show "forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter" as recited in claim 23. Appellants respectfully submit that the Figures do show the above recited limitation.

This limitation in claim 23 is described at page 12, lines 14-16 of the specification. "Another method of forming insulation liner 30 is CVD of a dielectric material, or a dielectric material precursor that deposits preferentially upon sidewall 50 of isolation trench 32." Thus, liner 30 in Figures 5A and 5B illustrates the deposition of a composition of matter as recited in claim 23.

Appellants therefore respectfully request that this objection to the drawings under 37 C.F.R. § 1.83(a) be overturned.

4. The claims 14-23, 25-27, and 31-40 do not need to be amended as suggested by the examiner to add an unnecessary nexus.

Claims 14-23, 25-27, and 31-40 stand objected to under 37 C.F.R. § 1.75(c) for being of improper dependent form for failing to further limit the subject matter of a previous claim. Particularly, the Office Action states that there is no nexus between claim 14's recited "material that is electrically insulative" (and similar recitations in the other rejected claims) and the other layers in the body of the claims. Appellants disagree.

In response to this rejection and with reference to Figures 8A and 8B, Appellants note that the Specification at page 15, lines 18-22 identifies an embodiment of the invention wherein a continuous (and electrically insulative) isolation structure includes parts of an isolation film, a pad oxide layer, an insulation liner, and a spacer. In other words, the claimed "material that is

electrically insulative" is not necessarily simply the "conformal layer" as required by the Examiner at page 4 of the Office Action.

Appellants therefore respectfully request the prompt removal of this objection.

5. Claim 23 should not be objected to under 37 C.F.R. § 1.75(c)

Claim 23 stands rejected under 37 C.F.R. § 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. Particularly, the Office Action states that the recitation of claim 23, "forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter" fails to limit, and contradicts, a recitation of claim 21, from which claim 23 depends: "said liner being confined within each said isolation trench and extending from a interface thereof." According to the Office Action, the deposition of a composition of matter cannot coincide with a liner "being confined within each said isolation."

In response, Appellants respectfully submit that the Examiner has failed to give sufficient weight to the well-known term "comprising" in claim 23. The term "comprising" is inclusive, not exclusive. *See e.g.* MPEP 8th ed. § 2111.03. In other words, even assuming, *arguendo*, the Examiner is correct in asserting that the act of depositing a composition of matter could not be confined within an isolation trench, that is not decisive because other unrecited acts could be performed to achieve a liner confined with each said isolation. Claim 23 does not, therefore, contradict claim 21.

Appellants therefore respectfully request that the objection to claim 23 under 37 C.F.R. § 1.75(c) be overturned.

6. Claim 34 should not be objected to because claim 34 is drafted correctly.

Claim 34 stands rejected for reciting the incorrect term. Particularly, the Office Action states that claim 34 should read: "a layer composed of polysilicon upon said ~~gate~~ oxide layer." (strikeout added to denote suggested deletion). Appellants disagree.

As acknowledged by the Examiner with reference to Figure 8B, gate oxide layer 44 is formed on semiconductor substrate 12 after exposing a surface on semiconductor substrate 12. As illustrate in Figure 8B, polysilicon island 24 is formed over gate oxide layer 24. Accordingly, Appellants respectfully assert that the objected to features of claim 34 are clearly demonstrated in the Specification and Drawings as filed, and no amendments are therefore necessary.

Appellants therefore respectfully request that the objection to claim 34 be overturned.

7. Claims 1 and 3-6 should not be rejected under 35 U.S.C. § 112, first paragraph.

Claims 1 and 3-6 stand rejected under 35 U.S.C. § 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Particularly, the Office Action alleges that there is no written description support for the recitation, "so as to define an upper surface contour of the conformal layer; and planarizing the conformal layer beginning with the upper surface contour of the conformal layer and extending at least to the first dielectric layer."

Initially, Appellants note that "drawings alone may provide a 'written description' of an invention as required by Sec. 112." *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1565, 19 U.S.P.Q.2d 1111, 1118 (Fed. Cir. 1991); *see also* M.P.E.P. (8th ed.) § 2163(II)(A)(3)((a).

Accordingly, Appellants respectfully assert the above rejected limitation finds support, in addition to the Specification, in Figures 6A and 6B of the application as filed.

Regarding the limitation, "so as to define an upper surface contour of the conformal layer," Appellant notes that isolation film 36 (one embodiment of the conformal layer) in Figure 6A has a contoured upper surface that is formed over the underlying structures. *See also* Specification at page 13, lines 22-24. Although this language is not explicitly recited in the Specification, such is not required, as noted above.

Regarding the subsequent limitation, "and planarizing the conformal layer beginning with the upper surface contour of the conformal layer and extending at least to the first dielectric layer," such is inherent in at least the definition of chemical mechanical planarization (CMP), which is described in the Specification as a preferred embodiment of the invention. *See* page 14, lines 14-17. It is well known by those skilled in the art that CMP is a partly mechanical, partly chemical process wherein a rotating polishing pad and a chemical slurry, for example, work together to flatten a material from upper surface downward. A conventional rotating pad used in CMP would necessarily start with the uppermost surface, here the upper surface contour.

Accordingly, Appellants respectfully assert that the application as filed contains a description in the specification that reasonably conveys to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the above claimed features of the invention. Appellants therefore respectfully request that the above rejection to claims 1 and 3-6 under 35 U.S.C. § 112, first paragraph be overturned.

8. Claims 14-27, 31-40, and 43 should not be rejected under 35 U.S.C. § 112, first paragraph.

Claims 14-27, 31-40, and 43 stand rejected under 35 U.S.C. § 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Particularly, the Office Action states that there does not appear to be a written description of the claim limitation "planarizing is performed in the absence of masking the conformal layer over each said isolation trench." Appellants respectfully disagree.

In the rejection the Examiner cites a section of the MPEP which states in part:

> The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection sought are set forth definitely, albeit negatively, the claim complies with the requirements of 35 U.S.C. 112, second paragraph.
>
> * * *
>
> The mere absence of a positive recitation is not basis for an exclusion.

MPEP 2173.05(i), 8th ed. Rev. 2, (emphasis added). Operations such as planarizing and selective removing are performed by chemical mechanical planarization or polishing (CMP) in embodiments of this invention that are disclosed in the Application. See, e.g., Application, p. 3, lines 25-26, p. 6, lines 1-3, p. 15, l. 4, p. 20, lines 15-17. The practice of CMP does not rely on masking, but it is known in contrast for its use to achieve an overall planar surface, sometimes referred to as global planarity. Appellants submit that this knowledge of a person of ordinary skill in the art, together with the disclosure in the Application of CMP for selective removing and/or planarizing, clearly delineate the bounds of the claimed invention.

Appellants therefore respectfully request that the above rejection to claims 14-27, 31-40, and 43 under 35 U.S.C. § 112, first paragraph be overturned.

9. Claim 23 should not be rejected under 35 U.S.C. § 112, first paragraph.

Claims 23 stands rejected for reciting under 35 U.S.C. § 112, first paragraph, "because the specification . . . does not reasonable provide enablement for the claims. Appellants respectfully disagree.

Particularly, the Examiner states that there is no enablement for "rounding the top edge of trench by deposition of a composition of matter." Office Action, page 7. However, that is not what claim 23 recites. Rather, claim 23 recites: "wherein forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter." It is claim 18, from which claim 23 depends, that recites, *inter alia*: "rounding the top edges of each of said isolation trenches." Claim 23 does not refer specifically to the above cited language from claim 18. In addition, as noted above, claim 23 uses the transitional phrase "comprising," not "consisting of," and so other recited actions can be performed within the scope of the claim. In other words, the Examiner is impermissibly importing into claim 23 limitations and requirements that are not there and basing a rejection based on these imported limitations.

The Examiner does not contend that there is no enablement for the recitation of claim 23: "wherein forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter." Appellants therefore respectfully request the overturn of this rejection.

10. Claims 9, 10, 12, 13, 26, and 27 Should not be Rejected Under 35 U.S.C. § 112, Second Paragraph.

Claims 9, 10, 12, 13, 26, and 27 stand rejected under 35 U.S.C. § 112, second paragraph, as failing to set forth the subject matter that Appellants regard as their invention. In particular, the office action states that the recitation of claim 9 (and similar language in 10, 12, 13, 26, and 27): "wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1," and the like contradicts the disclosure of the application as filed. Appellants respectfully disagree and submit that the above recited language does not contradict the language of the application as filed.

In context, and as read throughout the Specification as filed, it is clear that the isolation film 36 in the figures is etched slower than the insulator island. For example, at page 15, lines 11-15 the Specification states in part, "Reduced island 52 is preferably removed with an etch that is selective to isolation film 36 and spacer 28, leaving an isolation structure 48 that extends into and above isolation trench 32, forming a nail shaped structure having a head 54 extending above and away from isolation trench 32 upon an oxide layer 44." It is therefore clear that, as used in the specification, the term "selective to" indicates that a material is etched more slowly than other materials. Although the cited ratio of 2:1 at page 14, lines 14-25 may arguably be unclear if read in isolation, in context it is clear that substituting "slower" for "selective" is consistent with the specification. In other words, the hypothetically rephrased language: "A first preferred selectivity of an etch recipe used in the inventive method is in the range of about 1:1 to about 2:1, **slower** [selective] to isolation film 36 as compared to insulator island 22" is clear and consistent with the specification and Appellants previous arguments.

Hence, a correct reading of page 14, lines 14-25 of the specification is consistent with

claim 9 et al. in indicating that "planarization will be selective to isolation film 26."

Accordingly, Appellants respectfully request that the rejection of claims 9, 10, 12, 13, 26, and 27 under 35 U.S.C. § 112, second paragraph, be overturned.

11. Claims 1, 3-27, and 31-34 are unobvious over U.S. Patent No. 6,097,072 to Omid-Zohoor et al. ("the '072 patent") in view of U.S. Patent No. 5,387,540 to Poon et al. ("*Poon*").

Claims 1, 3-27, and 31-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,097,072 to Omid-Zohoor et al. ("the '072 patent") in view of U.S. Patent No. 5,387,540 to Poon et al. ("*Poon*"). Appellants respectfully submit that claims 1, 3-27, and 31-34 are unobvious over the '072 patent in combination with *Poon*.

Present claim 1 recites "filling each said isolation trench with a conformal layer . . . so as to define an upper surface contour of the conformal layer" and "planarizing the conformal layer beginning with the upper surface contour of the conformal layer and extending at least to the first dielectric layer and each said spacer." Support for this recitation can be found in the present application in Figures 6A and 6B.

In contrast, the method disclosed in the '072 patent relies on the deposition of a reverse-resist mask 368 over trench regions 356 (*see* the '072 patent, Fig. 3K, col. 4, *lines* 51-52) to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a reduced oxide layer 372 with ridges 373 (*see* the '072 patent, Fig. 3L, col. 4, *lines* 52-54). It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing (planarizing) until silicon nitride layer 344 is exposed (*see* the '072 patent, Fig. 3M, col. 4, *lines* 54-57, 59-61). Accordingly, the method disclosed in the '072 patent does

not teach or suggest planarizing the conformal layer "beginning with the upper surface contour of the conformal layer" as recited in claim 1.

Additionally, present claim 7 recites "filling each said isolation trench with a conformal layer . . . to a first thickness of the conformal layer relative to said spacers and said first dielectric layer" and "planarizing the first thickness of the conformal layer to a second reduced thickness." Support for this recitation can be found in the present application in Figures 6A and 6B.

As discussed above, the method disclosed in the '072 patent relies on the deposition of a reverse-resist mask 368 over trench regions 356 to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a reduced thickness oxide layer 372 with ridges 373. It is this reduced thickness oxide layer 372 that is subsequently treated by chemical-mechanical polishing (planarizing) until silicon nitride layer 344 is exposed. Accordingly, the method disclosed in the '072 patent does not teach or suggest "planarizing the first thickness of the conformal layer to a second reduced thickness" as recited in claim 7.

Further, claims 18 and 24-26 recite some form of planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, the '072 patent discloses a method that involves masking and etching a conformal layer prior to planarizing the layer.

Poon cannot cure the foregoing deficiencies of the '072 Patent. Thus, claims 1, 7, 18, and 24-26 would not have been obvious over the cited references.

Claims 3-6, 8-17, 19-23, and 27 depend from one of claims 1, 7, 18, and 26, respectively, and include the limitations recited therein. Accordingly, for at least the reasons presented above with respect to claims 1, 7, 18, and 26, claims 3-6, 8-17, 19-23, and 27 are not obviated by the '072 patent in view of *Poon*.

Present independent claim 31 recites "planarizing the *conformal layer* . . . to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (emphasis added).

In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse-resist mask 368 over trench regions 356 to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a remaining oxide layer 364 with ridges 373. It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing until silicon nitride layer 344 is exposed. Accordingly, the method disclosed in the '072 patent does not *planarize the conformal oxide layer* 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps.

Further, claim 31 recites that the planarizing is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, the '072 patent discloses a more complicated method that involves masking of a conformal layer.

Regarding claim 34, the '072 patent does not teach or suggest forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces. Consequently, the '072 patent does not teach or suggest the presently claimed method with the features recited in claim 34.

Poon cannot cure the foregoing deficiencies of the '072 Patent. Claims 32-34 depend from claim 31 and include the limitations recited therein. Accordingly, for at least the reasons

presented above with respect to claim 31, claims 32-34 are not obviated by the '072 patent in view of *Poon*.

Appellants therefore respectfully request that the rejection of claims 1, 3-27, and 31-34 under 35 U.S.C. § 103(a) be overturned.

12. Claims 35-40, 42, and 43 are Unobvious Over the '072 Patent in View of *Wolf, "Silicon Processing for the VLSI Era*."

Claims 35-40, 42, and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the '072 patent in view of Wolf, "*Silicon Processing for the VLSI Era*" (hereafter "*Wolf*") for the reasons stated on pages 26-33 of the Office Action. Appellants respectfully submit that claims 35-40, 42, and 43 are unobvious over the '072 patent in view of *Wolf*.

Claim 35 recites, *inter alia*, "forming a polysilicon layer upon said oxide layer." This polysilicon layer serves as an etch stop in various embodiments of the invention. *See e.g.* page 6, lines 15-17. The '072 patent has no such teaching or suggestion of this feature of the invention.

Additionally, claims 35, 38, and 42 recite some form of planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, as previously described, the '072 patent discloses a more complicated method that involves masking of a conformal layer and other steps.

In addition, present claim 43 recites, *inter alia* and with language variations in each claim, "planarizing the *conformal layer* ... to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (emphasis added). In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse-resist mask 368 over trench regions 356 to subsequently perform a wet or dry etch to partially remove oxide layer

364 and leave a remaining oxide layer 364 with ridges 373. It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing until silicon nitride layer 344 is exposed. Accordingly, the method disclosed in the '072 patent does not *planarize the conformal oxide layer* 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps.

Additionally, present claim 42 recites the use of a single etch recipe to form a planar upper surface from the conformal layer. In contrast, the method disclosed in the '072 patent, as previously noted, uses a multi-step method with different etch recipes to form a planar upper surface.

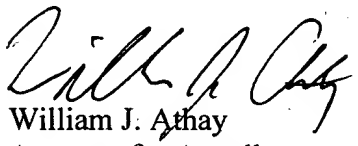
Wolf cannot cure the foregoing deficiencies of the '072 Patent. Claims 36, 37, 39, and 40 depend from one of independent claims 35 and 38, respectively, and include the limitations recited therein. Accordingly, for at least the reasons presented above with respect to claims 35 and 38, claims 36, 37, 39, and 40 are not obviated by the '072 patent in view of *Wolf*.

Appellants therefore respectfully request that the rejection of claims 35-40, 42, and 43 under 35 U.S.C. § 103(a) be overturned.

In view of the foregoing, Appellants respectfully request the Board to overturn the Examiner's rejections of the appealed claims.

Dated this 14th day of February 2005.

Respectfully submitted,



William J. Athay
Attorney for Appellants
Registration No. 44,515
Customer No. 022901

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APPENDIX: CLAIMS ON APPEAL

1. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer over and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

forming a liner upon a sidewall of each said isolation trench;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer, and said depositing is carried out to the extent of filling each said isolation trench and extending over said

spacers and over said first dielectric layer so as to define an upper surface contour of the conformal layer; and

planarizing the conformal layer beginning with the upper surface contour of the conformal layer and extending at least to the first dielectric layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other upper surfaces;

wherein the conformal layer comprises a material that is electrically insulative and extends continuously between and within said plurality of isolation trenches.

2. (cancelled)

3. A method according to Claim 1, wherein said liner is a thermally grown oxide of said semiconductor substrate.

4. A method according to Claim 1, wherein forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter.

5. A method according to Claim 1, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

6. A method according to Claim 1, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

7. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has an edge;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer and said depositing is carried out to the extent of filling each said isolation trench and extending over said spacers and over said first dielectric layer to a first thickness of the conformal layer relative to said spacers and said first dielectric layer;

planarizing the first thickness of the conformal layer to a second reduced thickness to form therefrom an upper surface for each said isolation trench that is co-planar to the other upper surfaces, wherein:

the conformal layer comprises a material that is electrically insulative and extends continuously between and within said plurality of isolation trenches;

said conformal layer and said spacers form said upper surface for each said isolation trench, each said upper surface being formed from said conformal layer and said spacer and being situated above said oxide layer; and

said first dielectric layer is in contact with at least a pair of said spacers and said oxide layer.

8. A method according to Claim 7, further comprising:

removing said oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

9. A method according to Claim 7, wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

10. A method according to Claim 9, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

11. A method according to Claim 7, wherein said upper surface for each said isolation trench is formed by the steps comprising:

chemical mechanical planarization, wherein said conformal layer, said spacers, and said first dielectric layer form a planar first upper surface; and

an etch that forms a second upper surface, said second upper surface being situated above said pad oxide layer.

12. A method according to Claim 11, wherein said etch uses an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

13. A method according to Claim 12, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

14. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon said oxide layer;

selectively removing said silicon nitride layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

forming a corresponding electrically active region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, said liner being confined preferentially within each said isolation trench and extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

filling each said isolation trench with a conformal second silicon dioxide layer, said conformal second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second silicon dioxide layer, and

said depositing is carried out to the extent of filling each said isolation trench and extending over said spacers and said silicon nitride layer; and

selectively removing said conformal second silicon dioxide layer and said spacers to form an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and being situated above said pad oxide layer, wherein a material that is electrically insulative extends continuously between and within said plurality of isolation trenches, and wherein said selectively removing is performed in the absence of masking the conformal second silicon dioxide layer over each said isolation trench.

15. A method according to Claim 14, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

16. A method according to Claim 14, wherein said liner is composed of silicon nitride.

17. A method according to Claim 15, further comprising:

removing said oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

18. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and

said depositing is carried out to the extent of filling each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein a material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein planarizing the conformal third layer to form therefrom said upper surface for each said isolation trench that is co-planar to the other said upper surfaces further comprises planarizing said conformal third layer and each said spacer to form therefrom said co-planar upper surfaces, and said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

19. A method according to Claim 18, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

20. A method according to Claim 18, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

21. A method according to Claim 18, further comprising, prior to filling each said isolation trench with said conformal third layer, forming a liner upon a sidewall of each said isolation trench, said liner being confined preferentially within each said isolation trench and extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate, and wherein said conformal third layer is composed of an electrically insulative material.

22. A method according to Claim 21, wherein said liner is a thermally grown oxide of said semiconductor substrate.

23. A method according to Claim 21, wherein forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter.

24. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and said depositing is carried out to the extent of filling each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

wherein the conformal third layer is an electrically insulative material that extends continuously between and within said plurality of isolation trenches;

wherein said upper surface for each said isolation trench is formed from said conformal third layer, said spacers, and said first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

25. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and said depositing is carried out to the extent of filling each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate;

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said oxide layer in contact with a pair of said spacers; and

selectively removing said third layer, said spacers and said layer composed of polysilicon to form a portion of at least one of said upper surfaces;

wherein a material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

26. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal third layer, and

said depositing is carried out to the extent of filling each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer by an etch using an etch recipe that etches said first dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from of about 1:1 to about 2:1 to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

wherein a material that is electrically insulative extends continuously between and within said plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

27. A method according to Claim 26, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

28-30. (cancelled)

31. A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a silicon nitride layer upon said polysilicon layer;

selectively removing said silicon nitride layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is in contact with said silicon nitride layer and said polysilicon layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding doped region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, each said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

rounding the top edges of said isolation trenches;

filling each said isolation trench with a conformal second layer, said second layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of filling each said isolation trench and extending over said spacers and over said silicon nitride layer; and

planarizing said conformal second layer and each of said spacers to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and is situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches;

wherein a material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

32. A method according to Claim 31, wherein each said liner is a thermally grown oxide of said semiconductor substrate, and wherein said conformal second layer is composed of an electrically insulative material.

33. A method according to Claim 31, wherein each said liner is composed of silicon nitride, and wherein said conformal second layer is composed of an electrically insulative material.

34. A method according to Claim 31, further comprising:

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate;

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and

selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces.

35. A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

selectively removing said first layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the exposed oxide layer at said plurality of areas, wherein an electrically insulative material extends continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of filling each said isolation trench and extending over said spacer and over said first layer;

having a top edge and said top edge being rounded; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer, wherein said planar upper surface is formed by planarizing in the absence of masking said second layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

36. The method as defined in Claim 35, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each said isolation trench.

37. The method as defined in Claim 36, wherein the doped trench bottom has a width, each said the isolation trench has a width, and the width of each said doped trench bottom is greater than the width of the respective isolation trench.

38. A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

selectively removing said first layer to expose said oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the oxide layer at said plurality of areas, wherein an electrically insulative material extends continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of filling each said isolation trench and extending over said spacer and over said first layer;

having a top edge and said top edge being rounded; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer, wherein said planar upper surface is formed by planarizing in the absence of masking said second layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

39. The method as defined in Claim 38, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of said isolation trenches.

40. The method as defined in Claim 39, wherein:

the doped trench bottom has a width;

each said isolation trench has a width; and

the width of each said doped trench bottom is greater than the width of the respective isolation trench.

41. (cancelled)

42. A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is curved; and

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

rounding the top edges of said isolation trenches;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of filling each of said isolation trenches and extending over said spacers and over said first layer; and

forming with a single etch recipe a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer;

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

43. A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is rounded; and

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, conformally filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of filling each of said isolation trenches and extending over said spacers and over said first layer; and

planarizing the conformal second layer and said first and second spacers of said respective first and second isolation structures to form a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches, and wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches.